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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION, HTC AMERICA, INC.,

Plaintiff,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 JF
(Related to 5:08-cv-05398 JF and 5:08-cv-00877 JF)

OPPOSITION TO PLAINTIFF HTC'S MOTION FOR SUMMARY JUDGMENT

Place: Courtroom 3, 5th Floor
Judge: Hon. Jeremy Fogel
Hearing: To Be Determined

[REDACTED]

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I. INTRODUCTION

Only by rewriting Defendants' Infringement Contentions can HTC conjure a scenario where the Contentions allegedly prove that HTC's accused products do not infringe the '749 patent. The actual combination of the excerpts Defendants' highlighted in ARM's Introduction to Thumb manual indicate to one skilled in the art how the accused products fetch multiple sequential instructions from memory in parallel, and supply them to the instruction register in a single memory cycle, as required by the claims of the '749 patent. Defendants' Contentions are thus sufficient, *Berger* does not apply, and HTC is not entitled to summary judgment.[1]

Similarly, HTC's argument for summary judgment of infringement of the '148 and '336 patents also fails. It assumes both that the Court accepts Plaintiffs' proposed improper limitations on the construction of the claimed "ring oscillator" based solely on the examiner's comment during the reexamination of the '148 patent, and then applies that construction to claim elements that are not a "ring oscillator," but are instead other specific claim terms, such as an "oscillator" or "variable speed clock." Both of those premises are wrong as a matter of law, and summary judgment should be denied.

II. LEGAL ARGUMENT

To defeat HTC's Motion for Summary Judgment ("Motion"), Defendants need only introduce evidence on which a reasonable jury could find infringement of the asserted claims of the '336 '749, and '148 patents. *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986). All alleged facts must be viewed in the light most favorable to Defendants, the non-movants. *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1304 (Fed. Cir. 1999). HTC's Motion for noninfringement is premised on the description of the accused products found in Defendants' Infringement Contentions (see Motion at 2:25-27), and the District Court opinion in *Berger v. Rossignol Ski Co., Inc.*, No. C 05-02523 CRB, 2006 WL 1095914 (N.D. Cal. April 25, 2006). In *Berger*, Judge Breyer granted summary judgment of noninfringement because the plaintiffs effectively conceded that their infringement contentions did not establish infringement, and Judge

[1] In the alternative, Defendants seek relief pursuant to Federal Rule of Civil Procedure 56(d) because HTC's Motion is premature where discovery is still in an early stage, and no discovery cut-off has been set.

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Breyer held that amendment of those contentions was not permitted in that case. The *Berger* case is neither similar in facts or infringement contentions and is not controlling or persuasive as to the present case, as shown both from the quotations and figures from the ARM document Defendants' cited in the '749 patent's Infringement Contentions, and from the expert declaration of Dr. Vojin Oklobdzija, submitted concurrently herewith.

Furthermore, HTC's Motion as to the '148 and '336 patents relies on three assumptions, none of which are correct. HTC is wrong when it seeks to limit the construction of "ring oscillator" to one that is "non-controllable," and "variable based on the environment" where such limitations do not appear in the patent claims and TPL made no such disclaimers. HTC is similarly wrong in attempting to apply such an improperly narrowed construction to claim terms that do not include the claimed "ring oscillator." Finally, HTC is wrong in assuming that an oscillator cannot infringe because it contains a voltage controlled oscillator or a current controlled oscillator.

Accordingly, HTC's Motion for summary judgment of noninfringement should be denied as to all three patents.

A. The Infringement Contentions Do Not Admit That The Accused Products Do Not Infringe The '749 Patent.

1. Claim 1 Of The '749 Patent Claims Supplying Multiple Sequential Instructions To The Instruction Register, Which Is Part Of The CPU.

Each asserted claim of the '749 patent contains the limitation that the microprocessor fetch multiple sequential instructions in parallel and supply them to the central processing unit ("CPU") during a single memory cycle. The parties agree, as evidenced by proposed constructions for a claim term, that these instructions are to be supplied to the CPU's instruction register during the same memory cycle in which they are fetched. Claim 1 of the '749 patent recites in part

> . . . means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle . . . .

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Joint Claim Construction Statement, Dkt. 189 Exh. B, Row 4. The parties agreed that the disclosed structure that corresponded to this §112 ¶6 claim term included at least the memory controller (118), instruction register (108), internal data bus (90), program counter (130) and internal address bus (136). *Id.* Thus, it is undisputed that the '749 patent in issue has the limitation that multiple sequential instructions are fetched from memory and supplied to the instruction register.

This is further confirmed by the language of the '749 patent's amended claim 1, which emerged from reexamination proceedings in the Notice to Issue Reexamination Certificate ("NIRC") on February 11, 2011 ." Declaration of Eugene Y. Mar, ("Mar Decl."), filed concurrently herewith, Ex. A. The full language of the claim is shown below, with the clarifying amendments underlined.[2] The amendments make clear that the means to fetch multiple sequential instructions from memory in parallel and supply them during a single memory cycle "comprises supplying the multiple sequential instructions in parallel to said *instruction register* during the same memory cycle in which the multiple sequential instructions are fetched." *Id.* (emphasis added).

[2] A microprocessor system, comprising a central processing unit integrated circuit, a memory external of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle, said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel, said central processing unit integrated circuit including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item;
wherein
the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded; and wherein
the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched. '749 Reexam Hist. 1/25/11 Amendment (Mar Decl., Ex. B), at 2.

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B. The Inventors Overcame The Transputer References And MacGregor By Disclaiming the Prior Arts' Failure To Fetch And Supply Multiple Sequential Instructions In A Single Memory Cycle.

The inventors overcame a rejection for anticipation by the two references from Edwards and May which described the "Transputer," a microprocessor designed by Inmos. The Transputer references disclosed fetching instructions into a prefetch buffer, however the Transputer was not capable of fetching and supplying the multiple instructions to the instruction register in a single memory cycle, as taught in the '749 patent. Pointedly, the Transputer references describe the instructions as being provided one at a time from the prefetch buffer to the instruction register, thus distinguishing the Transputer references from the '749 patent. The inventors traversed the rejection by noting that "[f]etching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation – the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'" '749 Reexam Hist., Chen Decl., Ex. 1 at 26 (Dkt. 294-1). While Edwards (May) disclosed fetching multiple instructions, it supplied them to the instruction register only one at a time, and therefore did not meet the claim.

Thus, the inventors disclaimed that fetching multiple instructions to a prefetch buffer and supplying them to the instruction register one at a time, and further that fetching and supplying to a prefetch buffer and then supplying to an instruction register, was not fetching and supplying in a single memory cycle. The inventors did not disclaim the mere presence of a prefetch buffer, as multiple sequential instructions could still be fetched and supplied to the instruction register in a single memory cycle by simply bypassing the prefetch buffer.[3]

C. The Infringement Contentions' Reference To The Introduction Of The Thumb State Of The ARM Core Specification Supports A Finding Of Infringement.

In cobbling together its summary judgment argument, HTC both misrepresents what was

[3] This was confirmed by the examiner who noted that "[r]egarding *claim* 1, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art to have the systems as claimed, further include the features of 'supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle the multiple instructions fetched'. This limitation is seen to clarify the function of the current invention, which is not expressly described in the closest cited prior art of the T414 Data Sheet, the May '948 reference, MacGregor, or Koopman. Thus, the claim, as presented in the amendment dated *1/25/2010*, is rendered as patentable." Mar Decl., Ex. A (NIRC) at 8.

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disclaimed in overcoming the Edwards and May references, and overstates Defendants' references to ARM's introductory documents cited in the infringement contentions. A closer look at both shows that the accused products do indeed infringe if they are capable of operating, and do operate as identified in the infringement contentions,[4] and *Berger* therefore does not apply. In any event, in opposing this motion Defendants seek and are entitled to further discovery on the operation of the accused products in Thumb state, where it is undisputed that the products can and do fetch multiple sequential instructions to the instruction register in one memory cycle.[5]

1. Plaintiffs Admit That The Accused Products Are Capable of Fetching Two Instructions At A Time From Memory And Supplying Them To The CPU In A Single Memory Cycle.

Unlike the situation in *Berger*, where the patent holder conceded that the infringement contentions did not establish infringement, Defendants here concede no such thing. With respect to the claim term at issue, [redacted]

[4] As HTC's Motion stipulates, the accused products are presumed to operate as set forth in the infringement contentions for purposes of this Motion. Motion at 2:25-26.

[5] While the Court can deny HTC's Motion on the merits because Defendants' Infringement Contentions are sufficient, Defendants also request relief in the alternative pursuant to Federal Rule of Civil Procedure 56(d). Any hearing on HTC's Motion should be continued until after Defendants have completed discovery on the design and operation of the accused products. As noted in *Klingele v. Eikenberg*, 849 F.2d 409, 412 (9th Cir. 1988), summary judgment is "generally disfavored where relevant evidence remains to be discovered. Summary judgment should be denied here where the parties are in the early stages of discovery, no depositions have even been noticed yet, at least 5 subpoenas are outstanding to suppliers of the microprocessors in HTC's accused products, and no discovery cut-off date has been set. Mar Decl., ¶ 13. As explained by Defendants' expert Dr. Oklobdzija, further document discovery is certain to bear fruit on the design and operation of the microprocessors in HTC's accused products. Declaration of Vojin Oklobdzija ("Oklobdzija Decl."), ¶21; Mar Decl., ¶ 16. Defendants also intend to obtain relevant evidence through depositions of engineers knowledgeable about the design and operation of the microprocessors in the accused products. *Id.* at ¶ 14.

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[redacted] This is wholly consistent with the claim language, as shown above, and, presuming the HTC products operate in accordance with the description set forth in the Infringement Contentions, is proof of infringement.

In light of the specific sections of the Infringement Contentions that show where multiple sequential instructions are fetched and supplied to the CPU's instruction register, *Berger v. Rossignol Ski Co., Inc.*, 2006 WL 1095914, does not apply, and HTC's Motion should be denied.

2. HTC's Motion Relies On Language From The ARM Document That Is Not Part of Defendants' Infringement Contentions.

[redacted] Thus, HTC's Motion is based on rewriting Defendants' Infringement Contentions and then arguing that the contentions as HTC has rewritten them do not infringe. Defendants have stated their Infringement Contentions and have cited to certain materials that support their contentions that the accused products practice the limitations of the '749 patent. Because HTC's argument is not limited to Defendants' Infringement Contentions, but goes beyond them to add language not cited or relied upon by Defendants to show infringement, it is improper. HTC's infringement contentions may insinuate that the accused products do not infringe the '749 patent, but

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Defendants' Infringement Contentions make no such concession.

As shown above in Section C.1, Figure 11 and the highlighted language in Example 2 confirm that the ARM architecture can fetch two 16-bit Thumb instructions which establishes one limitation of the infringement contentions, e.g., "multiple instructions." Not every citation has to establish every limitation in an asserted claim, and one skilled in the art would realize that in combination with Figure 11, the ARM Thumb state fetches two 16-bit instructions in parallel into the instruction register, and therefore infringes. Declaration of Dr. Vojin Oklobdzija ("Oklobdzija Decl."), submitted concurrently herewith; *see also* Section C.3, *infra*.

HTC is also incorrect when stating that the amendments during the re-examination are "immaterial to this motion." Motion at 4, n.4. These amendments are important because they are applicable to the extant patent and they further clarify the very limitation that is the subject of HTC's Motion. In their Reexamined Product Reports, Defendants also clarified that the claim term

> wherein the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched,

[redacted]

Remarkably, despite the fact that HTC's Motion alleges insufficiency in Defendants' contentions, HTC's argument relies on material Defendants did not cite in its contentions. *See* Mar Decl., Ex. D (Introduction to Thumb), "Example system configurations," pages 5–6 ("[t]he following three configurations demonstrate a Thumb-aware core in a system."). HTC's argument relies wholly upon language about the "latch" in Example 2 of the Introduction to Thumb, that was not highlighted by Defendants in the Infringement Contentions, while overlooking, as it must, Example 3 which illustrates the "final Thumb-aware step" where no "latch" is needed.

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Motion at 7-8. [redacted] HTC cannot gain summary judgment under *Berger* by cherry picking phrases and figures from a lengthy reference, and then arguing that HTC's own newly-created combination of statements never suggested by Defendants in their Infringement Contentions, does not satisfy the claims.

3. Dr. Oklobdzija Concurs That Defendants' Infringement Contentions Prove Infringement.

The sufficiency of infringement contentions are determined by their meaning to one possessing ordinary skill in the art, and here, Defendants' expert Dr. Vojin Oklobdzija, concurs that Defendants' contentions articulate a theory of infringement that is consistent with the patent claims, prior art and accused products.

As Dr. Oklobdzija explains, assuming the HTC accused products act as described in the reference materials cited in Defendants' Infringement Contentions for the '749 patent, one of ordinary skill in the art would conclude that the accused products infringe. As an initial point, all of the accused products contain an embedded ARM microprocessor core. Oklobdzija Decl., ¶ 7. As ARM's documents cited in the Infringement Contentions confirm, an ARM microprocessor core executes the ARM instruction set, which includes Thumb instructions. *Id*. Thumb instructions are 16 bits, half the width of 32-bit ARM instructions, and expand the ARM instruction set to include a mixture of both 32-bit and 16-bit instructions. *Id*., Mar Decl., Ex. D, at 7-8.

[redacted] The Introduction to Thumb document

[6] As previously discussed, the amendment of claim 1 in reexamination clarified that (1) the multiple sequential instructions are fetched and supplied into the instruction register in the CPU, and (2) that the multiple sequential instructions are supplied in parallel to the instruction register.

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discusses how to take advantage of the ARM core's ability to fetch and supply multiple 16-bit instructions to the instruction register. *Id.*, ¶ 9, Introduction to Thumb at 7. Since one word is described as 32-bits and instructions are fetched one word at a time, two 16-bit instructions are therefore stored in one 32-bit instruction word in instruction memory. *Id.* Dr. Oklobdzija confirms that this is clear to one skilled in the art [redacted] Thus, fetching a 32-bit instruction word that contains two 16-bit instructions from instruction memory and storing that word in the instruction register constitutes supplying two instructions to the instruction register "in parallel," as required by Claim 1 of the '749 patent. *Id.*, ¶ 9. The fact that the same word being fetched is supplied to the instruction register without further fetches means that it is fetched and supplied during a "single" memory cycle.

HTC seeks a finding of noninfringement due to the alleged presence of a prefetch buffer in Defendants' Infringement Contentions, and HTC's argument accordingly requires the accused product have a prefetch buffer to avoid infringement. However, Defendants' Infringement Contentions neither describe nor rely on any structure that could be deemed a prefetch buffer that would require two fetches to supply a fetched word from memory to the instruction register. [redacted] As such, HTC's argument relies on manufactured evidence of a prefetch buffer, and therefore should be rejected.

Dr. Oklobdzija further explains that storing the multiple sequential instructions (fetched in parallel from memory) in the instruction register is shown in Figure 11 of the Introduction to Thumb document. *Id.*, ¶10. Because the standard ARM instructions are 32-bits wide, the instruction register that stores the standard ARM instructions is also 32-bits wide. *Id.* When in Thumb state, the instruction register will hold two Thumb instructions, as shown in Figure 11, which are decoded during the decode cycle. *Id.* The decode stage receives inputs from the instruction register, which are supplied over the 32-bit wide instruction bus. *Id.* [redacted]

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Defendants' Infringement Contentions are sufficiently detailed to indicate to one skilled in the art how the accused products fetch multiple sequential instructions in parallel from memory, and supply them to the instruction register in a single memory cycle, as explained by Dr. Oklobdzija. This is further evidence showing why HTC's Motion should be denied.

III. THE INFRINGEMENT CONTENTIONS FOR THE '148 AND '336 PATENTS ARE LIKEWISE SUFFICIENT.

HTC's Motion devotes four paragraphs to its unsubstantiated theory that none of its accused products can infringe the '148 or '336 patents because "the claimed oscillator, ring oscillator and variable speed clock must be, among other things, non-controllable." Mot. at 9:15-16. HTC's theory assumes both that the Court accepts Plaintiffs' proposed improper limitations on the construction of the claimed "ring oscillator" based solely on the examiner's comment

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during the reexamination of the '148 patent, and then applies that construction to claim elements that are not a "ring oscillator," but are instead other specific claim terms, such as an "oscillator" or "variable speed clock." Both of those premises are wrong. HTC then posits that, because the Infringement Contentions for the '336 and '148 patents identify a voltage or current controlled oscillator as a structure meeting the "'ring oscillator' related elements",[7] there can be no infringement because a voltage controlled oscillator ("VCO") "could be controlled by voltage or current." Mot. at 10. This of course assumes that a VCO could not infringe because Plaintiffs' construction is correct. Again, this is wrong, and HTC's Motion should be denied.

A. TPL Did Not Disclaim The Talbot Oscillator Based on Controllability.

1. TPL Did Not Disclaim A Controlled Ring Oscillator In Distinguishing Talbot.

HTC's argument that the claimed ring oscillator must be "noncontrollable" and "variable based on the environment" relies merely on three sentences from a record that includes two reexaminations, and ignores the context from an examiner's interview summary regarding the Talbot reference during the '148 patent's reexamination:

> Continuing, the patent owner further argued that the reference of Talbot does not teach [sic] of a "ring oscillator." The patent owner discussed features of a ring oscillator, such as being ***non-controllable***, and being ***variable based on the environment***. The patent owner argued that ***these features distinguish over what Talbot teaches***.

[7] HTC's suggestion that "ring oscillator," "oscillator," and "variable speed clock" should be construed identically tramples the doctrine of claim differentiation, which dictates that different claims with different language have different meaning and should not be inferred to have the same construction. Even if the on chip ring oscillator were the only embodiment of the variable speed clock, which it is not, the Federal Circuit has "**expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment**." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005); *see also Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) (internal citations and quotation marks omitted) ("[E]ven where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction."). Here, during the prosecution of the '336 patent, the inventors clearly described that the ring oscillator is "an example of the oscillator recited in the claims, the clock rate of which varies in the same way as a function of one or more device parameters associated with the integrated circuit substrate." '336 Pros. Hist., Amendment 7/7/97, (Mar Decl., Ex. E), at TPL0001930. Thus, in both the specification, the prosecution of the patent, and the claims themselves, the patentee exhibited a clear intent ***not*** to limit the claim scope.

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'148 Reexam Hist. Interview Summary, 2/12/08 (Chen Claim Construction Responsive Declaration, Ex. C (Dkt. 244-3)(emphasis added).

HTC ignores, as it must, that the patent owners promptly filed a written response to the summary that distinguished Talbot not on the basis that its oscillator was controlled, but on the basis that the oscillators that were being controlled by the control circuitry were not ring oscillators. *Id.* 2/21/2008 '148 Reexam Hist., Chen Claim Const. Decl., Ex. H (Dkt. 244-8), at 11. HTC's argument is flatly inconsistent with any agreement by the patent owner that control of the Talbot's oscillator was even remotely relevant to the point of novelty over Talbot.

In detail, the patent owners filed a response that directed the examiner's attention to the two oscillator implementations of Talbot's Figures 3 and 4, pointing out that "neither [was] a ring oscillator." *Id.* "As the sole inventor of the cited reference, Talbot presumably possesse[d] at least ordinary skill in the art, yet Talbot did not characterize either of the disclosed oscillators as ring oscillators." *Id.* The examiner then agreed that it was unclear whether the "specific features" of the Talbot oscillator circuits "actually ma[d]e a ring oscillator." '749 Reexam Hist 6/25/08 Office Action (Mar Decl. Ex. F), at TPL0019232. The subsequent allowance over Talbot was therefore not about the voltage control aspects of Talbot, but about whether the controlled oscillators were ring oscillators. As such, disclaimer does not apply. *See Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324-25 (Fed. Cir. 2003) ("We have … declined to apply the doctrine of prosecution disclaimer where the alleged disavowal of claim scope is ambiguous." (collecting cases)).

2. The Oscillator In Talbot's Figure 3 Is Also Not A Ring Oscillator Pursuant To Judge Ward's Claim Construction In The Texas Litigation.

Not only did Talbot not characterize the disclosed oscillator in Figure 3 as a ring oscillator, it is also not a ring oscillator as construed by Judge Ward in the prior Texas litigation. Judge Ward's construction of "ring oscillator" requires, to oscillate, "a multiple, odd number of inverting logic stages connected in a loop." (Markman Order, Chen Claim Const. Decl., Ex. A, at 11 (Dkt. 244-1).) In direct contrast to the ring oscillator that Judge Ward construed, Defendants' expert Dr. Oklobdzija explains that Talbot does not require multiple odd numbers of inversion

stages to oscillate. The oscillator in Talbot's Figure 3 is capable of oscillating using only the Schmitt trigger (52), in combination with the capacitor 50 (and 54). Declaration of Vojin G. Oklobdzija at ¶¶ 16-17. *See also* Talbot, (Chen Claim Const. Decl., Ex. B) at col.8:15-21 (Dkt. 244-2) ("as the capacitor 50 discharges the voltage at the node 53 will fall and when it reaches the other trigger value for the Schmitt trigger 52, the output of the Schmitt trigger will again change state. Thus, an oscillating output signal will be provided at the output 56 of the voltage controlled oscillator circuit and the oscillation will be sustained.").

A Schmitt trigger does not change the output of a signal (from LOW to HIGH, or from HIGH to LOW) until the input voltage meets a certain threshold level. Oklobdzija Decl., ¶ 17. The capacitors 50 (and 54) are used to charge and discharge the voltage needed to attain the threshold voltage used to "trigger" the Schmitt trigger. *Id.* Because a Schmitt trigger employs different threshold voltages for triggering the transitions from HI to LOW, and LOW to HIGH, these unequal threshold voltages allow oscillation to be maintained when combined with a capacitor. *Id.* Contrary to the circuit described in Talbot, a single stage of a ring oscillator with an output connected to an input will not oscillate, but will instead remain at a stable voltage level. *Id.* at ¶ 19. Thus, a person of ordinary skill in the art would understand that Figure 3 of Talbot is not a ring oscillator since it requires only the Schmitt trigger and capacitor to oscillate, and does not require multiple odd stages of inversions. *Id.* Accordingly, Talbot does not disclose a ring oscillator as construed by Judge Ward.

3. The Claimed Ring Oscillator Is Controllable.

Not only is HTC's selective analysis of the reexamination history flawed, it is contradicted by the patent specification, which states that the ring oscillator's "frequency is determined by the parameters of temperature, voltage, and process." '336 patent at 16:59-60. If the frequency can be a function of voltage, or vary according to the voltage applied to it, the ring oscillator is by definition able to be controlled by at least voltage, as well as temperature and process. It is undisputed for purposes of this Motion that a PLL indicates the presence of an on-chip ring oscillator, associated with either a voltage controlled oscillator or a current controlled oscillator. Because HTC's motion for summary judgment rests wholly on its argument that the

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claimed ring oscillator must be "non-controllable," which is contradicted by the reexamination history and the specification, HTC's noninfringement argument must fail.

IV. CONCLUSION

For this Court to grant HTC's Motion for summary judgment of noninfringement of the '749 patent based on insufficient infringement contentions, it must accept two erroneous premises. First, it must conclude that the patent owners disclaimed a prefetch buffer in reexamination, even though the record shows that the patent owners actually disclaimed the Transputer references at issue for failing to fetch and supply multiple sequential instructions in a single memory cycle. And second, the Court must agree that HTC can rewrite Defendants' actual Infringement Contentions to go beyond the language and figures that Defendants relied upon in showing how the accused products infringe. Because neither of these premises is supported in law or fact, the Motion should be denied as to the '749 patent.

HTC's Motion for summary judgment of noninfringement of the '336 and '148 patents is similarly flawed, and should also be denied. The patent owners did not disclaim controlled oscillators in distinguishing Talbot, making HTC's proposed claim construction of "ring oscillator" wrong as a matter of law.

Finally, because discovery is still in its early stages in this matter, Defendants respectfully request that in the alternative, the Court grant relief under Federal Rule of Civil Procedure 56(d) to allow discovery of infringement to be completed prior to ruling on HTC's Motion.

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Dated: April 26, 2011

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I represent that concurrence in the filing of this document has been obtained from each of the other signatories which shall serve in lieu of their signatures on this document.

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